

CLAIMS

1. A programmable logic circuit comprising:
 - a plurality of unit logic circuits connected in parallel;
 - 5 an input signal control section that supplies input signals received from outside to the plurality of unit logic circuits; and
 - 10 an output signal control section that supplies output signals of the plurality of unit logic circuits to outside,
 - each of the plurality of unit logic circuits comprising:
 - 15 a logic operation section that performs predetermined logic operation on the input signals and generates data, said logic operation section having functions that are changeable based on first setting information;
 - 20 a data processing section that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on second setting information, and provides the data to the output signal control section as output signals;
 - 25 a storage section that stores the first and second setting information; and
 - a memory control section that takes control by receiving jump setting information, reading out

either the first or the second setting information
of the storage section based on the jump setting
information and providing the setting information
to the logic operation circuit and the data
5 processing section,

wherein each of the plurality of unit logic circuits
sequentially changes some or all of the functions of the
logic operation section and the data processing section
based on the first and second setting information read
10 out sequentially from the storage section and carries
out predetermined operations of a sequential circuit.

2. A programmable logic circuit comprising:

a plurality of unit logic circuits connected in
15 parallel;

an input signal control section that supplies input
signals received from outside to the plurality of unit
logic circuits; and

an output signal control section that supplies
20 output signals of the plurality of unit logic circuits
to outside,

each of the plurality of unit logic circuits
comprising:

a logic operation section that performs
25 predetermined logic operation on the input signal
and generates data, said logic operation section
having functions that are changeable based on first

setting information;

a data processing section that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on the second setting information, and provides the data to the output signal control section as output signals;

a storage section that stores the first and second setting information; and

10 a memory control section that receives stopping setting information and controls stopping between the logic operation section and the data processing section based on the stopping setting information,

15 wherein each of the plurality of unit logic circuits sequentially changes some or all of the functions of the logic operation section and the data processing section based on the first and second setting information read out sequentially from the storage section and carries

20 out predetermined operations of a sequential circuit.

3. The programmable logic circuit according to one of claims 1 and 2, wherein the logic operation section further comprises a logic cell that performs predetermined logic operation on the input signals and generates data, said logic cell having functions that are changeable based 25 on the first setting information.

4. The programmable logic circuit according to one of claims 1 to 3, wherein the data processing section further comprises a cross-connecting switch that generates data
5 by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on the second setting information.

5. The programmable logic circuit according to claim
10 4, wherein the data processing section comprises a flip-flop that holds the data from the cross-connecting switch and supplies the data to the output signal control section as the output signals.

15 6. A programmable logic circuit comprising:
a plurality of unit logic circuits connected in parallel;
an input signal control section that supplies input signals received from outside to the plurality of unit
20 logic circuits;
a connecting section that connects one unit logic circuit in the plurality of unit logic circuits and another unit logic circuit neighboring the one unit logic circuit in physical arrangement; and
25 an output signal control section that supplies output signals of the plurality of unit logic circuits to outside,

each of the plurality of unit logic circuits comprising:

5 a logic operation section that performs predetermined logic operation on one of the input signal and data from the another neighboring unit logic circuit and generates data, said logic operation section having functions that are changeable based on first setting information;

10 a data processing section that carries out arrangement, duplication and inversion processing on the data from the logic operation section based on second setting information, generates data, and provides the data to the output signal control section as output signals;

15 a storage section that stores the first and second setting information; and

20 a memory control section that takes control by receiving jump setting information, reading out either the first or the second setting information of the storage section based on the jump setting information and provide the setting information to the logic operation circuit and the data processing section,

25 wherein each of the plurality of unit logic circuits sequentially changes some or all of the functions of the logic operation section and the data processing section based on the first and second setting information read

out sequentially from the storage section and carries out predetermined operations of a sequential circuit.

7. A programmable logic circuit comprising:

5 a plurality of unit logic circuits connected in parallel;

an input signal control section that supplies input signals received from outside to the plurality of unit logic circuits;

10 a connecting section that connects one unit logic circuit and another unit logic circuit neighboring the one unit logic circuit in physical arrangement in the plurality of unit logic circuits; and

15 an output signal control section that supplies output signals of the plurality of unit logic circuits to outside,

each of the plurality of unit logic circuits comprising:

20 a logic operation section that performs predetermined logic operation on one of the input signal and data from the another neighboring unit logic circuit and generates data, said logic operation section having functions that are changeable based on the first setting information,;

25 a data processing section that carries out arrangement, duplication, and inversion processing on the data from the logic operation

section based on the second setting information, and generates data and provides the data to the output signal control section as the output signals;

5 a storage section that stores the first and second setting information; and

 a memory control section that receives stopping setting information and controls stopping between the logic operation section and the data 10 processing section based on the stopping setting information,

 wherein each of the plurality of unit logic circuits sequentially changes some or all of the functions of the logic operation section and the data processing section 15 based on the first and second setting information read out sequentially from the storage section and carries out predetermined operations of a sequential circuit.

8. The programmable logic circuit according to claim 20 7, wherein the logic operation section further comprises a logic cell that performs predetermined logic operation on the input signals and generates data, said logic cell having functions that are changeable based on the first setting information.

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9. The programmable logic circuit according to one of claims 6 to 8, wherein the data processing section further

comprises a cross-connecting switch that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on the second setting information.

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10. The programmable logic circuit according to claim 9, wherein the data processing section comprises a flip-flop that holds the data from the cross-connecting switch and supplies the data to the output signal control
10 section as the output signals.

11. A programmable logic circuit comprising:

a plurality of unit logic circuits connected in parallel;

15 an input signal control section that supplies input signals received from outside to the plurality of unit logic circuits; and

an output signal control section that supplies output signals of the plurality of unit logic circuits
20 to outside, the input signal control section comprising:

a section that supplies a control signal to the plurality of unit logic circuits based on the input signal;
and

25 a section that supplies index information to the plurality of unit logic circuits at the time of receiving an index designation signal,

each of the plurality of unit logic circuits

comprising:

a logic operation section that performs predetermined logic operation on the input signal and generates data, said logic operation section having
5 functions that are changeable based on any of the first setting information;

a data processing section that carries out arrangement, duplication, and inversion processing on the data from the logic operation section based on any
10 of the second setting information, generates data and provides the data to the output signal control section as the output signals;

a storage section storing the first and second setting information; and

15 a memory control section that stores a lead position address indicating the lead position of storage position addresses of the first and second setting information at the storage section based on one of the control signal and index information at the time of receiving one of
20 the control signal and the index information,

wherein each of the plurality of unit logic circuits sequentially changes some or all of the functions of the logic operation section and the data processing section based on either the first or second setting information
25 read out sequentially from the storage section based on the lead position address stored in the memory control section and carries out predetermined operations of a

sequential circuit.

12. The programmable logic circuit according to claim 11, wherein the logic operation section further comprises 5 a logic cell that performs predetermined logic operation on the input signals and generates the data, said logic cell having functions that are changeable based on the first setting information.

10 13. The programmable logic circuit according to claim 11, wherein the data processing section further comprises a cross-connecting switch that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on 15 the second setting information.

14. The programmable logic circuit according to claim 13, wherein the data processing section comprises a flip-flop that holds the data from the cross-connecting 20 switch and supplies the data to the output signal control section as the output signals.

15. A programmable logic circuit comprising:
a plurality of unit logic circuits connected in
25 parallel;
a connecting section that connects one unit logic circuit and another unit logic circuit neighboring the

one unit logic circuit in physical arrangement in the plurality of unit logic circuits;

an input signal control section that supplies input signals received from outside to the plurality of unit logic circuits; and

an output signal control section that supplies output signals of the plurality of unit logic circuits to outside,

the input signal control section comprising:

10 a section that supplies a control signal to the plurality of unit logic circuits based on the input signal; and

a section that supplies index information to the plurality of unit logic circuits at the time 15 of receiving an index designation signal, and each of the plurality of unit logic circuits comprising:

20 a logic operation section that performs predetermined logic operation on the input signal or data from the another neighboring unit logic circuit and generates data, said logic operation section having functions that are changeable based on any of the first setting information;

25 a data processing section that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on any of the second setting

information and provides the data to the output signal control section as the output signals;

a storage section that stores the first and second setting information; and

5 a memory control section that stores a lead position address indicating the lead position of storage position addresses of the first and second setting information at the storage section based on one of the control signal and index information
10 at the time of receiving one of the control signal and the index information,

wherein each of the plurality of unit logic circuits sequentially changes some or all of the functions of the logic operation section and the data processing section
15 based on either the first or second setting information read out sequentially from the storage section based on the lead position address stored in the memory control section and carries out predetermined operations of a sequential circuit.

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16. The programmable logic circuit according to claim 15, wherein the logic operation section further comprises a logic cell that performs predetermined logic operation on the input signals and the data from the another
25 neighboring unit logic circuit and generates the data, said logic cell having functions that are changeable based on the first setting information.

17. The programmable logic circuit according to claim
15, wherein the data processing section further comprises
a cross-connecting switch that generates data by carrying
5 out arrangement, duplication and inversion processing
on the data from the logic operation section based on
the second setting information.

18. The programmable logic circuit according to 17,
10 wherein the data processing section further comprises
a flip-flop that holds the data from the cross-connecting
switch and supplies the data to the output signal control
section as the output signals.